IN THE CLAIMS:

Please amend the claims as indicated below.

1. (Currently Amended) A cache memory, comprising:

a plurality of sets of cache frames for storing information from main memory;

a thrashing detector for determining when one or more of said sets are a thrashed set; and

a selector for identifying one or more additional frames to augment said thrashed set, wherein said one or more additional frames and said thrashed set are at the same memory hierarchical level as said cache.

2. (Original) The cache memory of claim 1, wherein said thrashing detector evaluates a miss rate of a set.

3. (Original) The cache memory of claim 2, wherein said thrashing detector further comprises a miss counter and an access counter.

4. (Original) The cache memory of claim 2, wherein said miss rate of a set is determined by comparing a number of misses experienced during a given number of accesses.

5. (Original) The cache memory of claim 1, further comprising a mapper that transforms a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more additional sets.

6. (Original) The cache memory of claim 1, wherein said selector identifies said one or more additional frames to augment said thrashed set using an access rate of said additional frames.

7. (Original) The cache memory of claim 1, wherein said selector identifies said one or more additional frames to augment said thrashed set using a position in an address space of said additional frames.

8. (Original) The cache memory of claim 1, wherein said one or more additional frames are shared with said thrashed set.

9. (Original) The cache memory of claim 1, further comprising a mechanism for disassociating said one or more additional sets from said thrashed set when the additional sets are no longer needed to decrease thrashing.

10. (Currently Amended) A method for reducing thrashing in a cache memory, said method comprising the steps of:

storing information from main memory in a plurality of sets of cache frames;

detecting when one or more of said sets are a thrashed set; and

identifying one or more additional frames from said plurality of sets to augment said thrashed set, wherein said one or more additional frames and said thrashed set are at the same memory hierarchical level as said cache.

11. (Original) The method of claim 10, wherein said detecting step further comprises the step of evaluating a miss rate of a set.

12. (Original) The method of claim 11, wherein said miss rate is obtained using a miss counter and an access counter.

13. (Original) The method of claim 11, wherein said miss rate of a set is determined by comparing a number of misses experienced during a given number of accesses.

14. (Original) The method of claim 10, further comprising the step of transforming a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more additional sets.

15. (Original) The method of claim 10, wherein said identifying step further comprises the step of identifying said one or more additional frames to augment said thrashed set using an access rate of said additional frames.

16. (Original) The method of claim 10, wherein said identifying step further comprises the step of identifying said one or more additional frames to augment said thrashed set using a position in an address space of said additional frames.

17. (Original) The method of claim 10, wherein said one or more additional frames are shared with said thrashed set.

18. (Original) The method of claim 10, further comprising the step of disassociating said one or more additional sets from said thrashed set when said additional sets are no longer needed to decrease thrashing.

19. (Currently Amended) A cache memory, comprising:

means for storing information from main memory in a plurality of sets of cache frames;

means for detecting when one or more of said sets are a thrashed set; and

means for identifying one or more additional frames from said plurality of sets to augment said thrashed set, wherein said one or more additional frames and said thrashed set are at the same memory hierarchical level as said cache.

20. (Original) The cache memory of claim 19, wherein said means for detecting thrashing evaluates a miss rate of a set.

21. (Original) The cache memory of claim 20, wherein said means for detecting thrashing further comprises means for counting frame misses counter and frame accesses.

22. (Original) The cache memory of claim 20, wherein a miss rate of a set is determined by comparing a number of misses experienced during a given number of accesses.

23. (Original) The cache memory of claim 19, further comprising means for transforming a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more additional sets.

24. (Original) The cache memory of claim 19, wherein said means for identifying identifies said one or more additional frames to augment said thrashed set using an access rate of said additional frames.

25. (Original) The cache memory of claim 19, wherein said means for identifying identifies said one or more additional frames to augment said thrashed set using a position in an address space of said additional frames.

26. (Original) The cache memory of claim 19, further comprising means for disassociating said one or more additional sets from said thrashed set when the additional sets are no longer needed to decrease thrashing.

27. (Currently Amended) An integrated circuit, comprising:

a cache memory having a plurality of sets of cache frames for storing information from main memory;

a thrashing detector for determining when one or more of said sets are a thrashed set; and

a selector for identifying one or more additional frames to augment said thrashed set, wherein said one or more additional frames and said thrashed set are at the same memory hierarchical level as said cache.

28. (Original) The integrated circuit of claim 27, wherein said thrashing detector evaluates a miss rate of a set.

29. (Original) The integrated circuit of claim 27, further comprising a mapper that transforms a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more additional sets.

30. (Original) The integrated circuit of claim 27, further comprising a mechanism for disassociating said one or more additional sets from said thrashed set when the additional sets are no longer needed to decrease thrashing.